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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/622,734	11/27/2000	Keisuke Koga	YAO-432US	2803

7590 12/03/2002

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EXAMINER
MONDT, JOHANNES P

ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 12/03/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/622,734	KOGA, KEISUKE	
	Examiner	Art Unit	
	Johannes P Mondt	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on *19 August 2002* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6 and 9-16* is/are rejected.

7)☒ Claim(s) *7,8 and 17* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *5* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

The Final Rejection formulated in Office Action No. 10 mailed 11/04/2002 is herewith replaced by the present Office Action.

Information Disclosure Statement

The examiner has considered the item previously lacking in the file, namely Kawaguchi (JP401061953A).

Response to Amendment

Amendment B filed 8/19/2002 and entered as Paper No. 9 forms the basis for the present Office Action. For comments on Applicant's Remarks in said Amendment B please be referred to "Response to Arguments" below.

Response to Arguments

1. Applicant's arguments filed 8/19/2002 have been fully considered but they are not persuasive. With regard to the objections against the specification, the examiner thanks Applicant for the clarification and withdraws the objection. However, the examiner has elaborated and repeated his objections against claims 7 and 8 (and also against newly added claim 17 for the same reasons) (see below). With regard to the drawings: the examiner withdraws his objections in view of the newly submitted compliance with the required drawing corrections. With regard to the substantial

amendments of independent claims 1, 4 and 5 and consequently of their dependent claims 2, 3 and 6, comments on Remarks by Applicant are restricted to those pertaining to rejected claims 9-13, other than to draw Applicant's attention to the fact that the traverse of claims 1, 4 and 5 are all exclusively based on the newly introduced limitations added through Amendment B.

With regard to claim 9, in Figure 5 the control or gate electrode 35 (cf. line 4 of "Solution" in the Abstract and Figure 4) is obviously hidden from view by the extraction electrode 36 (line 6 of "Solution" in the Abstract and Figure 4) exactly because it has the same orientation and lateral location as said extraction electrode. For that reason Hirano et al do disclose gate electrodes positioned symmetrical in a plane with respect to the cathode portion of the field emission electron source portion as specified by claim 9. Although Applicant does not concede that it would be obvious to combine the references (Kuriyama et al and Hirano et al) no specific traverse is provided based on the obviousness argument presented by the examiner.

With regard to claim 10: Applicant's traverse is based on that of the rejection of independent claim 9, which traverse has been discussed above.

Claim Objections

1. ***Claims 7, 8 and 17*** are objected to because of the following informalities:

In claim 7 the phrase "the shield electrode is provided in such a manner as to cover the channel region of the field effect transistor portion which is not covered with the gate electrode" should be replaced by "the shield electrode is provided in such a

manner as to cover the channel region of the field effect transistor portion which is not covered with the gate electrode, while the potential of said shield electrode is made to be equal to that of the substrate". The objection aims to (a) comply with what Applicant intends in view of the disclosure, specifically page 40, lines 28-30 for example; while (b) avoiding the application of prior art showing only a gate electrode but with the defining properties of both the shield electrode and the gate electrode.

Applicant is respectfully reminded that appropriate correction is required.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. ***Claims 1, 5, 14 and 16*** are rejected under 35 U.S.C. 103(a) as being unpatentable over Kuriyama et al (5,550,435) in view of Kojima (5,965,921).

With regard to claim 1: Kuriyama et al teach (cf. Figure 3) a field emission type electron source device (cf. title and abstract) comprising:

a field emission electron source portion including an extraction electrode 2 (cf. column 4, line 38) provided on a p-type silicon substrate 5 (cf. column 4, line 39) via an insulating film 3 (cf. column 4, line 38) and having an opening portion (located around 1, see Figure 3) at a position corresponding to a region

where a cathode is provided; and a cathode portion provided on the p-type silicon substrate and at a position corresponding to the opening portion of the extraction electrode; and

an n-channel field effect transistor portion (comprising IGFET gate 8, channel between source 6 and drain 4/6; cf. column 4, line 41) provided on the p-type silicon substrate, corresponding to the field emission electron source portion, wherein:

the field emission electron source portion is provided in a drain region 4/6 (cf. column 4, lines 39-40) of the field effect transistor portion; and a control voltage is applied to a gate electrode 8 (cf. column 4, line 41) of the field effect transistor portion to control a field emission current from the field emission source portion;

the drain region includes at least two wells 4 and 6 having different impurity concentrations (4 is n-doped and 6 is n+ doped silicon) (cf. column 4, lines 45-46); and

of the at least two wells, one well having a low impurity concentration is provided at an end of the drain (said drain being to the left of the channel between drain and source; cf, Figure 3) which contacts the channel region of the field effect transistor portion.

Kuriyama et al do not necessarily teach the further limitation that the well having low impurity concentration is provided around a circumference of the other well having a higher impurity concentration. However, as is evidenced by

Kojima, it is well known in the art of field effect transistors with insulated gate that the rated voltage can be improved by surrounding the heavily doped drain region by a lightly doped drain region so as to further reduce the gate-drain capacitance; see column 9, lines 1-40 and column 11, line 54 – column 12, line 8). Motivation to include the teaching by Kojima in this regard is the desirability to improve the rated voltage for any insulated gate field effect transistor, including the IGFET in the invention by Kuriyama et al. The inventions can be easily combined through slightly extending the lightly doped drain region. Success in implementing the combination of the teaching by Kojima and the invention by Kuriyama et al can therefore be reasonably expected.

With regard to claim 5: the gate insulation film between the p-silicon substrate 5 and IGFET gate 8 as taught by Kuriyama et al is thinner than the first insulating film 3 (see Figure 3) while the first insulating film is provided between the extraction electrode 2 and the p-type silicon substrate 5, while the gate insulating film is buried with the first insulating film. Therefore, with reference to the comments made on claim 1, it is concluded that for exactly the same reasons as given for claim 1 claim 5 is unpatentable over Kuriyama et al in view of Kojima.

With regard to claims 14 and 16: the extraction electrode as taught by Kuriyama et al is provided in a region above the drain region and away from an interface between regions of different impurity concentrations, namely the region in the upper right corner of Figure 3 marked "Grid Electrode").

3. ***Claims 2-3*** are rejected under 35 U.S.C. 103(a) as being unpatentable over Kuriyama et al and Kojima as applied to claim 1, and further in view of Akamatsu et al (5,396,096).

As explained above, claim 1 is unpatentable over Kuriyama et al in view of Kojima.

Kuriyama et al nor Kojima necessarily teach the further limitation of claim 2. However, the use of two different impurity elements having different thermal diffusivities or diffusion speeds in the silicon substrate has long been known and applied in the art of field effect transistors, as witnessed by Akamatsu et al, who teach the thermal diffusion of phosphorus and arsenic whose diffusion coefficients are different from each other, phosphorus having a high thermal diffusivity, arsenic having a relatively low thermal diffusivity in the silicon substrate 10 (this remark pertains to claim 3), thus obtaining a heavily doped part and a lightly doped part of the drain (cf. column 11, line 66 – column 12, line 3).

It is well known that the purpose of LDD (lightly doped drain) implementation is the avoidance of hot electron carrier effects (cf. column 11, lines 53-55 in loc. cit.) while the purpose of using different impurities distinct in having different thermal diffusivities is one of obvious convenience: a single heating process establishes two diffusion regions. It is concluded that there is thus motivation to combine the references and that the long-standing success of thermal diffusion for impurity doping combined with the very

different thermal diffusivities of phosphorus and arsenic justify a reasonable expectation of success.

4. ***Claims 4 and 15*** are rejected under 35 U.S.C. 103(a) as being unpatentable over Kuriyama et al (5,550,435) in view of Kojima (5,965,921) and Kawaguchi (JP401061953A) (as listed in the Information Disclosure Statement of Paper No. 5).

With regard to claim 4: Kuriyama et al teach (cf. Figure 3) a field emission type electron source device (cf. title and abstract) comprising:

a field emission electron source portion including an extraction electrode 2 (cf. column 4, line 38) provided on a p-type silicon substrate 5 (cf. column 4, line 39) via an insulating film 3 (cf. column 4, line 38) and having an opening portion (located around 1, see Figure 3) at a position corresponding to a region where a cathode is provided; and a cathode portion provided on the p-type silicon substrate and at a position corresponding to the opening portion of the extraction electrode; and

an n-channel field effect transistor portion (comprising IGFET gate 8, channel between source 6 and drain 4/6; cf. column 4, line 41) provided on the p-type silicon substrate, corresponding to the field emission electron source portion, wherein:

the field emission electron source portion is provided in a drain region 4/6 (cf. column 4, lines 39-40) of the field effect transistor portion; and a control voltage is applied to a gate electrode 8 (cf. column 4, line 41) of the field effect

transistor portion to control a field emission current from the field emission source portion.

Kuriyama et al do not necessarily teach the further limitation that the gate electrode of the field effect transistor portion has a shape such that a portion of the gate electrode nearer the drain region has a total width wider than a total width of a portion of near the source region. However, in order to prevent hot carrier generation in a depletion layer of the drain junction, Kawaguchi teaches a gate electrode 1 in a MOS transistor to be wider on the drain side 2 than on the source side 3 (see "Purpose" and "Constitution" in Abstract). Motivation to include the teaching of Kawaguchi in this regard in the invention by Kuriyama et al stems from the circumstance that suppression of said hot carrier generation would increase the withstand voltage, which is in line with the objective of Kuriyama et al (see column 1, line 55 – column 2, line 11).

Furthermore, all that is necessary for a combination of the inventions is a widening of the gate near the drain. Therefore, reasonable expectation of success is justified.

With regard to claims 15: the extraction electrode as taught by Kuriyama et al is provided in a region above the drain region and away from an interface between regions of different impurity concentrations, namely the region in the upper right corner of Figure 3 marked "Grid Electrode").

5. ***Claim 6*** are rejected under 35 U.S.C. 103(a) as being unpatentable over Kuriyama et al and Kojima as applied to claim 5 above, and further in view of Hirano et al (JP409063467A).

As detailed above, Kuriyama et al anticipate Claim 5; however, they do not necessarily teach the further limitation of Claim 6. Nevertheless, it would have been obvious to use thermal oxidation to produce the insulating film as it is understood in the art that silicon dioxide is an excellent insulating film generally in semiconductor field effect device technology while it is economically produced, given the silicon substrate suitable to provide the fuel, while Hirano et al teach the use of thermal oxidation for the more specific purpose of sharpening the tip of the cathode portion of the field emission electrode source portion of their cold cathode device (see [0034] and title and abstract). Motivation to combine stems from the requirement of a micropoint of the electron emitter taught by Kuriyama et al (see their claim 1 for instance). Combinability of the inventions by Kuriyama et al and Hirano et al is obvious in view of the efficiency of producing said tip and gate insulating film together in this manner. Reasonable expectation of success of the combination of said inventions follows from the fact that no new steps are introduced at any stage.

6. ***Claims 9 and 11-13*** are rejected under 35 U.S.C. 103(a) as being unpatentable over Kuriyama et al (5,550,435) and Hirano et al (JP409063467A). As explained above, Kuriyama et al essentially teach the limitations of claim 9 up to and including line 14. Although Kuriyama et al do not specifically teach the limitation concerning the drain

(lines 15-18), Hirano et al teach a field emission type electron source device with substantially circular borders of the drain with the emitter in the center, as seen from Figure 5, such that the drain is provided in and surrounded by the source region. Also, Figure 5 shows the gate electrode of the field effect transistor to be positioned substantially symmetrical in a plane with respect to the cathode portion of the field emission electron source portion, because the control electrode is just and exactly underneath the electrode depicted in Figure 5 in plan view (please view jointly Figures 4 and 5, and be referred to control electrode 35 as the gate electrode; also please be referred to section [0029] of Hirano et al concerning the relevance for a MOSFET of the invention of Hirano et al as further illustrated by cross-sectional Figure 8 of a MOSFET). A lack of symmetry of the configuration consisting of the emitter, the drain region as surrounded by the source region, and the gate would necessarily permit the occurrence of asymmetries in the potentials and currents, thereby necessarily and obviously leading to a lower breakdown voltage of the semiconductor portions of the device for the same level of electron flux.

With regard to claim 11: it is inherent in any channel, as defined in the art of field effect transistors, that it is a conduit between source and drain. Therefore, an outer portion of the drain region must contact the channel region of the field effect transistor portion. Furthermore, the above-mentioned symmetry (claim 9) implies that the inner portion of the source region has concentric circles.

With regard to claim 12: combination of Figures 4 and 5 implies, with the symmetry discussed under claim 9, that the gate electrode provided between source and drain has at least a part that has a shape of a symmetrical circular arc.

With regard to claim 13: It is understood by those skilled in the art that minute gate voltages suffice to substantially change the conductivity in the channel, whence the very essence of the applicability of field effect transistors, while, as taught by Kuriyama et al, extraction voltages of the order of 10^7 V/cm are involved for electron emission (cf. column 2, lines 55-60).

7. ***Claim 10*** is rejected under 35 U.S.C. 103(a) as being unpatentable over Kuriyama et al and Hirano et al as applied to claim 9 above, and further in view of Bergonzoni (4,968,639). As detailed above, claim 9 is unpatentable over Kuriyama et al in view Hirano et al, neither of whom necessarily teach the further limitation defined by claim 10. However, the inclusion of p-type conductive layers in an n-type drain has long been known by those skilled in the art of lightly-doped drain type field effect transistors as a means to combat punch-through, as witnessed by Bergonzoni, who teaches p-type layers 13' in n-type drain and source regions 31 (cf. column 2, lines 45-63). Because the purpose of the lightly doped drain regions is relevant to the aim of Kuriyama et al to gain better control of emission the motivation to combine the references is clear. Implementation is simply achieved in the manner indicated by Bergonzoni (loc. cit.) by lightly doped the upper region of the substrate comprising the step of thermal diffusion already pertinent to the device of claim 9 because of the existence of course and drain

regions. As only an additional step similar to the step of producing source and drain is involved in the implementation of the relevant aspect of Bergonzoni, expectation of success is justifiably deemed reasonable.

Allowable Subject Matter

8. ***Claims 7, 8 and 17*** would be allowable subject to compliance with the request for appropriate action as stated in the abovementioned objections.

9. The following is a statement of reasons for the indication of allowable subject matter: Shielding electrodes in the art of field emission type electron sources with field effect transistor, so as to cover a part of the channel not covered by the gate electrode while having the same potential as the substrate, said shielding electrodes being made of the same material as the gate, have not been found in the Prior Art to date, nor has any reason surfaced as to why such shielding electrodes should be obvious.

Conclusion

10. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not

mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Johannes P Mondt whose telephone number is 703-306-0531. The examiner can normally be reached on 8:00 - 18:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan J Flynn can be reached on 703-308-6601. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7722 for regular communications and 703-308-7724 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

JPM
November 29, 2002

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